IN THE CLAIMS:

This version of the claims replaces all previous versions and listings.

Claim 1. (canceled)

2. (Currently Amended) A high speed interface device, comprising:

a DRAM unit for generating first clock and first clock bar signals which do not have a phase difference from a main clock signal, and second clock and second clock bar signals having 90° phase difference from the first clock and clock bar signals during a write operation, storing an inputted 4 bit data in one period of the main clock signal according to the first and second clock and clock bar signals, synchronizing the stored data with data strobe signals according to the first and second clock and clock bar signals during a read operation, and outputting a 4 bit data during one period of the main clock signal;

a controller for transmitting a command, address signal and data signal synchronized with the main clock signal to the DRAM unit during the write operation, and receiving data signals from the DRAM unit during the read operation; and ~~The device according to claim 1~~, further including a circuit for generating the data strobe signals, comprising:

a first delay unit for receiving the first clock signal;

a first buffer unit connected between an output terminal of the first delay unit and an output terminal for outputting a first data strobe signal;

a second delay unit for receiving the second clock signal; and

a second buffer unit connected between an output terminal of the second delay unit and an output terminal for outputting a second data strobe signal.

3. (Currently Amended) A high speed interface device, comprising:

a DRAM unit for generating first clock and first clock bar signals which do not have a phase difference from a main clock signal, and second clock and second clock bar signals having 90° phase difference from the first clock and clock bar signals during a write operation, storing an inputted 4 bit data in one period of the main clock signal according to the first and second clock and clock bar signals, synchronizing the stored data with data strobe signals according to the first and second clock and clock

bar signals during a read operation, and outputting a 4 bit data during one period of the main clock signal; and

a controller for transmitting a command, address signal and data signal synchronized with the main clock signal to the DRAM unit during the write operation, and receiving data signals from the DRAM unit during the read operation ~~The device according to claim 1~~, wherein the DRAM unit comprises:

a third buffer unit for receiving the main clock signal and a main clock bar signal from the controller;

a DLL unit for delay locking output signals from the third buffer unit, and generating the first clock and first clock bar signals;

a fourth buffer unit for buffering and outputting the first clock and first clock bar signals from the DLL unit, and transmitting the first clock and first clock bar signals to the DLL unit;

a phase shift unit for receiving the first clock and first clock bar signals from the DLL unit, and generating the second clock and second clock bar signals;

a fifth buffer unit for receiving and buffering output signals from the phase shift unit;

a write latch unit for storing inputted write data according to the first and second clock and first and second clock bar signals; and

a read latch unit for storing read data from a read sense amp according to the first and second clock signal and first and second clock bar signals.

4. (Original) The device according to claim 3, wherein the write latch unit comprises:

a first latch unit for storing a first data from an input buffer according to the first clock signal during the write operation;

a second latch unit for storing a second data from the input buffer according to the second clock signal during the write operation;

a third latch unit for storing a third data from the input buffer according to the first clock bar signal during the write operation; and

a fourth latch unit for storing a fourth data from the input buffer according to the second clock bar signal during the write operation.

5. (Original) The device according to claim 3, wherein the read latch unit comprises:

a first latch unit for storing a first data from the read sense amp unit according to the first clock signal during the read operation;

a second latch unit for storing a second data from the read sense amp unit according to the second clock signal during the read operation;

a third latch unit for storing a third data from the read sense amp unit according to the first clock bar signal during the read operation; and

a fourth latch unit for storing a fourth data from the read sense amp unit according to the second clock bar signal during the read operation.

6. (New) A high speed interface type device for a memory device, comprising :

a first buffer part receiving a main clock signal;

a DLL circuit part receiving an output of the first buffer part and outputting an internal clock signal being synchronized with the main clock signal;

a second buffer receiving the internal clock signal and outputting a first clock signal a second clock signal;

a phase shift part receiving the internal clock signal of the DLL circuit part and shifting the phase of the internal clock signal by 90 degree;

a third buffer receiving an output of the phase shift part and outputting a third clock signal a fourth clock signal; and

a latch part receiving the first to fourth clock signals,

wherein the phase of the first clock signal is in synchronism with the phase of the main clock signal, the phase of the second clock signal is in synchronism with a phase of a signal being generated by inverting the main clock signal,

the phase of the third clock signal is more lagged by 90 degree than the phase of the main clock signal,

the phase of the fourth clock signal is in synchronism with a phase of a signal being generated by inverting the third clock signal, and

data latched in the latch part is outputting or inputting in synchronism with the rising edge of the first to fourth clock signals.

7. (New) The high speed interface type device according to claim 6, wherein the latch part includes a first latch being controlled by the first clock signal, a second latch being controlled by the

second clock signal, a third latch being controlled by the third clock signal, and a fourth latch being controlled by the fourth clock signal.

8. (New) The high speed interface type device according to claim 6, wherein data outputting from the latch part or inputting to the latch part in synchronous with the first to forth clock signals, during one period of the main clock signal, are 4 bits.

9. (New) The high speed interface type device according to claim 6, wherein a duty ratio of the first clock signal is 50%.